High Performance Circuits in 0.18 um SiGe BiCMOS Process for Wireless Applications

Peihua Ye, Bipul Agarwal, Madhukar Reddy, Larry Li, Jackie Cheng, Paul C Mudge, Evan McCarthy, and Stephen L Lloyd

Conexant Systems Incorporated, 4311, Jamboree Road, K09-950, Newport Beach, CA 92660, USA

Abstract — **Silicon Germanium Bipolar CMOS (SiGe BiCMOS) process technology is gaining increasing popularity for RF circuits in wireless applications due to high performance, low cost, high yield and higher levels of integration with mixed signal and digital CMOS circuits. Four test circuits were designed and fabricated in Conexant's 0.18 um SiGe BiCMOS process to evaluate the performance benefits provided by this state of the art process technology. The RF performance achieved in this process clearly makes this a process of choice for future RFIC products**

I. Introduction

Due to shrinking form factors of handsets, there is a great need for higher levels of integration in RF circuits for cellular phones. Also, the need for lower cost RFICs constantly requires evaluation of Silicon based processes which provide an additional advantage of integration of digital baseband circuits on to the RFIC. So far, the performance achievable by Silicon based processes (purely bipolar or BiCMOS) is inferior when compared with GaAs based discrete devices. This is especially true in cellular phones designed for CDMA standard where some phone manufactures prefer GaAs based discrete front ends over Si based front ends due to lower current consumption and better overall front end performance. However, with the evolution of SiGe processes, the performance achievable by SiGe RF circuits is making them an attractive option for RFICs. In order to prove the performance of the state of the art SiGe BiCMOS process, four test circuits were designed and fabricated in Conexant's 0.18 um SiGe BiCMOS process [1]. These circuits are a) low noise amplifier, b) down conversion mixer, c) power amplifier driver and d) prescaler. The circuits were chosen as they would best capture the RF performance capabilities of the process.

II. Process Technology

The features of the technology include three types of SiGe NPN transistors (high speed, standard and high voltage), poly resistors, 0.18 um CMOS, high-Q metal-insulator-metal (MIM) capacitors, varactors, and high Q inductors. The open base breakdown voltage (BVCEO) is 2.0 V for the high speed SiGe NPN, 3.0V for standard SiGe NPN and 6 V for the high voltage SiGe NPN. The cut-off frequency (ft) is 120 GHz for high speed SiGe NPN, 75 GHz for the standard SiGe NPN, and 35 GHz for the high voltage SiGe NPN. The test chip was fabricated with six layers of metal. The substrate resistivity is 8 ohm-cm. More details about this process technology can be found in [1].

III. Test Circuits

Four circuits were chosen to evaluate the RF performance capability of this process. These circuits were not designed to a specific cellular phone requirement. Instead the design goal was to optimize the performance of each circuit for the most difficult parameter while maintaining acceptable performance on other parameters. The design and performance of the circuits will be described in the following order, a) low noise amplifier, b) down conversion mixer, c) power amplifier driver, and d) prescaler.

A. Low noise Amplifier (LNA)

A simplified schematic of the LNA is shown in Fig. 1. It is a common emitter single stage amplifier, and it is designed for lowest noise figure possible in the US PCS band (1.96 GHz).

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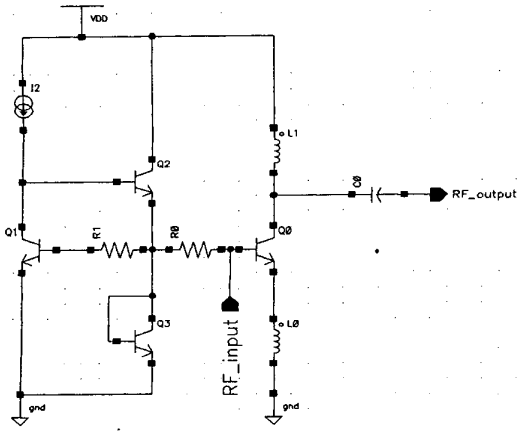

Figure 1. Simplified schematic of the LNA

The emitter length of the SiGe bipolar was scaled to get the optimum Noise Figure (NF), Gain, and input return loss (S11). Bias currents are generated through an on-chip band-gap reference voltage and an external bias resistor. Table 1 lists the measured results at Vcc=3V and various DC currents.

TABLE I

LNA measurements at 1.96 GHz and Vcc=3 V

Ic (DC, mA)	6.9	2.75
IIP3 (dBm)	10.3	12.6
Gain (dB)	16.9	16.2
NF (dB)	1	0.99
S11 (dB)	-12	-10
S22 (dB)	-19	-16

Noise figure (NF) was measured on HP8970B noise meter, and a 0.2dB input trace loss was deducted. The input third intercept points (IIP3) were measured with tones at 1.96 GHz and 1.961GHz. Fig. 2 shows the output power of fundamental and IM3 versus input power at Ic (DC)=6.9mA.

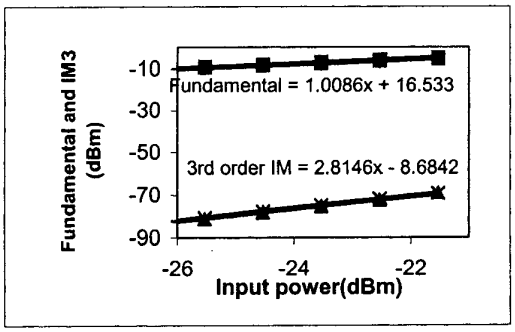

Figure 2. Fundamental and IM3 power versus input power

B. Downconversion mixer

A simplified schematic of double balanced mixer is

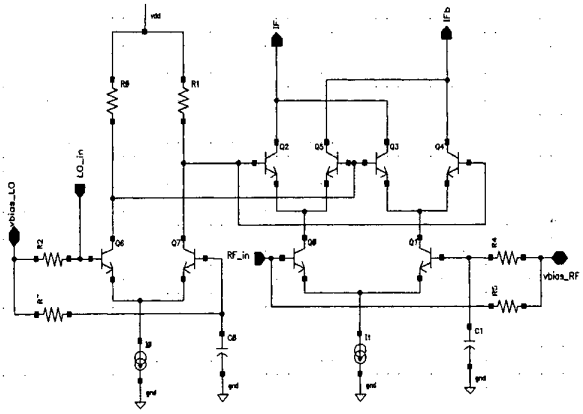

Figure 3. Simplified schematic of a double balance mixer

shown in Fig. 3. The LO signal at 1.75 GHz is fed single ended to the LO buffer which converts it to differential limiting LO signals. A single ended RF signal is fed to the input transconductance stage, and is converted to differential signals. The differential RF signals are fed to the switching quad that is hard switched by limiting LO signals. The down converted IF and IFb signals flow out of the open collectors of the switching quad, and are filtered with an external LC tank.

Table II lists the simulation results of the mixer. Measurements are not available currently due to a layout error on the test chip that prevents DC biasing of the mixer.

TABLE II

Mixer simulations, RF at 1.96 GHz, LO at 1.75 GHz and Vcc= 3.0 V

	Simulations
Ic (DC), mA	14
Gain, dB	10.7
IIP3, dBm	6.4
Noise Figure, dB	7.3
LO port, S22, dB	-11
RF port, S11, dB	-15

C. Power Amplifier Driver

A simplified schematic of driver is shown in Fig. 4. It is a single stage, common emitter amplifier with emitter degeneration.

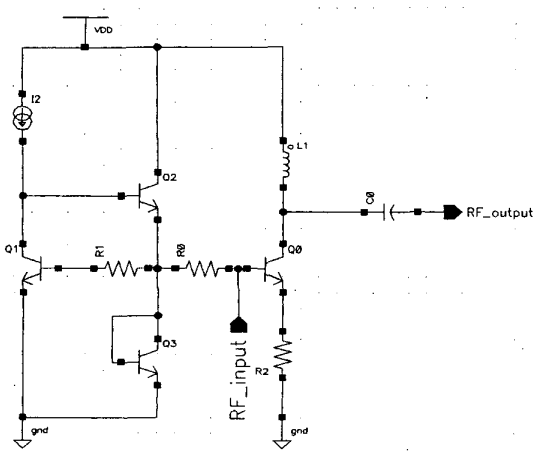

Figure 4. Simplified schematic of a PA driver circuit

With proper DC biasing, the driver operates in class AB mode. In this mode, the average current in the driver goes up with the input power level, thereby maintaining acceptable IM3/IM5 products even at higher power levels. This is particularly useful for minimizing current consumption in transmitters where the output power can vary over a wide range.

The Adjacent Channel Power Ratio (ACPR) measurements were taken at 1.88GHz with an offset of 1.25MHz. The DC power supply is 3V, and DC current is 4.8mA. Table III lists the measurement results at output power=7, 8, 9 dBm. Fig. 5 shows ACPR and IM3 (dBc) versus output power, and Fig. 6 shows the power gain of the driver versus output powers.

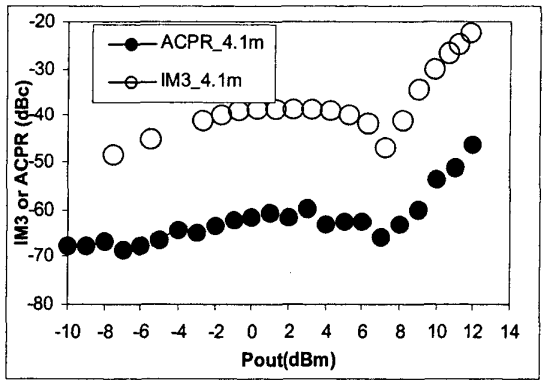

Figure 5. IM3 and ACPR versus output power.

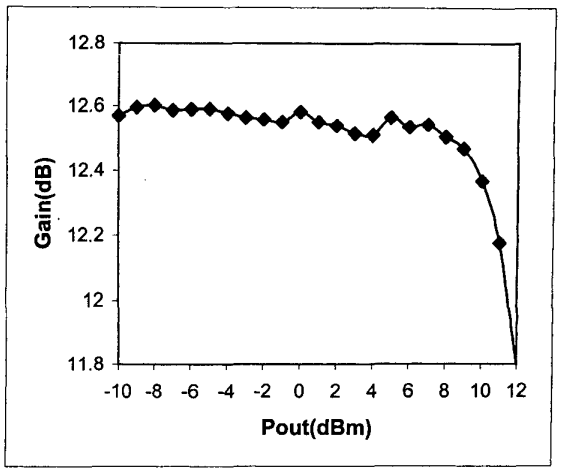

Figure 6. Power gain versus output power.

TABLE III
Measurement results of the driver at 1.88 GHz

Pout (dBm)	Gain (dB)	ACPR (dBc)	IM3 (dBc)	I_average (mA)
7	12.5	-65	-42	8.13
8	12.5	-63	-40	8.74
9	12.4	-56	-33	9.62

D. Dual-modulus prescaler

The dual-modulus prescaler was designed to divide a 2.75GHz frequency signal by either 32 or 33 depending on whether the control voltage is set to high or low. The prescaler input sensitivity is as low as –23 dBm, and the output voltage swing of the divided signal is 3V. The dual-modulus prescaler consists of a DC bias block, a synchronous divide by 4/5 divider, and an asynchronous divider by 8. The synchronous divide by 4/5 circuit contains two NAND gates and three master-slave flip-flops operating at the input frequency. The asynchronous divide by 8 circuit contains three flip-flops and three AND gates.

Fig. 7 shows a typical schematic of a flip-flop used in the prescaler. Table IV lists simulation and measurement results of the maximum input frequency at which the prescaler operates and the current consumption. It shows that the prescaler can work up to 3.8GHz at Vcc=3.3V and 3.3GHz at Vcc=3V. The total current is 0.96 mA for both Vcc=3.3V and 3V.

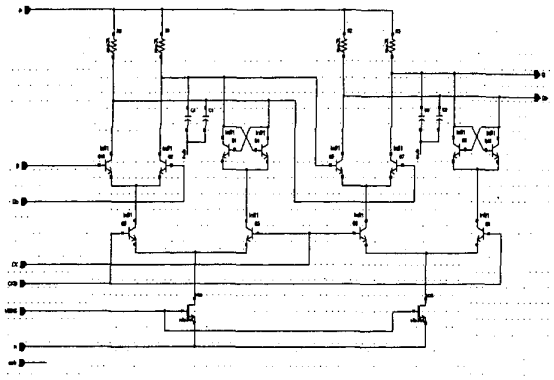

Fig. 7. Schematic of a flip-flop used in the prescaler.

TABLE IV
Measured and simulated maximum operating frequency (GHz)

	Measured	Simulated
At Vcc=3.3V	3.8 GHz	4.2 GHz
At Vcc=3 V	3.3GHz	3.8 GHz

Typically, the prescaler and the preceding buffer consume most of the current in a frequency synthesizer as these circuits operate with signals at RF frequency. The power consumption of this prescaler is about 45% lower than that of BiCMOS prescalers operating under similar conditions. This implies that frequency synthesizers will benefit from the SiGe BiCMOS process not only in terms of lower current consumption but also due to a smaller die area of the digital counters in 0.18 um CMOS.

V. Conclusion

Four RF test circuits were designed and fabricated in Conexant's 0.18 um SiGe BiCMOS process. These circuits demonstrate excellent RF performance at low current consumption. The performance shown by these circuits along with the integration levels achievable in 0.18 um SiGe BiCMOS process clearly make it a strong contender for RF circuits in wireless applications. With further process developement, 0.18 um SiGe BiCMOS has shown even better performance [2] than the process utilized for these circuits. With such advances in SiGe process technology, SiGe BiCMOS will be utilized for most of the future wireless RFIC products.

Acknowledgement

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